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EXAMINER	
BEVERIDGE, RACHEL E	
ART UNIT	**PAPER NUMBER**
1725	

DATE MAILED: 12/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/722,432	KWARK ET AL.	
	Examiner	Art Unit	
	Rachel E. Beveridge	1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *25 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7-13,15,17,19,20,23,24,27,31 and 32* is/are rejected.

7)☒ Claim(s) *4,6,14,16,18,21,22 and 28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 32 is objected to because of the following informalities: new claim 32 recites, "bonding wired" on line 2, which the examiner suggests amending to recite, --bonding wires.-- Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 7, 9, 12, 19, 24, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (US 6,084,295).

With respect to claim 1, Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-54). Horiuchi teaches a plurality of bonding wires (20) with conductive wire and electro-insulation coating for electrically connecting the circuit board (5) to the semiconductor chip (10) (column 2, lines 1-9). Horiuchi also discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33).

With regard to claim 2, Horiuchi further teaches predetermined distances between each wire and shows wires subsequently above each other in figure 1.

Regarding claim 3, Horiuchi also shows wires in a predetermined configuration alongside one another in figures 7(a) and 8.

Regarding claim 5, Horiuchi discloses "it is possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and/or thickness of the resin coating *32* covering the conductive wire" (column 5, lines 29-33).

With respect to claim 7, Horiuchi teaches the resin coating (32) to cover the bonding section and an electro-conductive resin (34) used for shielding (column 6, lines 14-17). Figure 3 also shows an epoxy type coating (30) on a gold wire (28) to be the bond wire (20) connecting the signal between semiconductor and circuit board.

With respect to claim 9, Horiuchi also shows wires in a predetermined configuration alongside one another in figures 7(a) and 8.

With regard to claim 12, Horiuchi's figure 3 shows a round bonding wire.

Regarding claim 19, the examiner interpreted high to be any value for dielectric constant of the insulating material due to the lack of relation to a low value and lack of specified values for a high dielectric constant. Horiuchi discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33) and that an electro-conductive resin (34) is capable of easily shielding the semiconductor chip (10) (column 5, lines 34-37). Horiuchi also discloses the lack of risk of a short-circuit between the bonding wires (20) even though they are shielded with electro-conductive resin (34) because the electrode terminals and bonding section between the wires (20) and pads (22) are covered with electro-insulation resin (32) (column 5, lines 37-44).

With respect to claim 24, Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-54). Horiuchi teaches a plurality of bonding wires (20) with conductive wire and electro-insulation coating for electrically connecting the circuit board (5) to the semiconductor chip (10) (column 2, lines 1-9). Horiuchi also discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33).

Regarding claim 27, Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-54). Horiuchi teaches a plurality of bonding wires (20) with conductive wire and electro-insulation coating for electrically connecting the circuit board (5) to the semiconductor chip (10) (column 2, lines 1-9). Horiuchi also discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33). Horiuchi further teaches predetermined distances between each wire and shows wires subsequently above each other in figure 1.

Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Notani et al. (US 5,294,897).

Notani discloses the reduction of the reflection of high frequency signals caused by the mismatching of characteristic impedances in the transmission line (column 6, lines 6-9). Notani also discloses a transmission line with continuous transmission between the lines and the circuit package substrate (column 5, lines 34-40).

Furthermore, Notani shows a plurality of bonding wires in figures 1(a), 4(b), 6, 7, 8, and 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 5 above, and further in view of Chia et al. (US 2004/0182911 A1).

Horiuchi teaches epoxy as insulation but lacks disclosure of the type of epoxy used for the invention. Chia teaches wire bonding utilizing an insulating liquid (112), more specifically using ultra-violet light-cured epoxies (Chia et al., page 1, paragraph [0021], lines 3-4). Therefore, it would have been obvious to one of ordinary skill the art at the time of the invention to modify the wire bonding method of Horiuchi to utilize the ultra-violet light-cured epoxy of Chia in order to electrically insulate the bonding wires and attach them to the package in any desired sequence without causing package defects (Chia et al., page 2, paragraph [0026], lines 3-7).

Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Steranko et al. (US 3,840,169).

With respect to claim 10, Horiuchi teaches dispensing wires for bonding but lacks disclosure of co-dispensing a plurality of bonding wires. However, Steranko discloses bonding multiple wires to a circuit board continuously (abstract, lines 1-9) as shown in figure 1. Regarding claim 11, Horiuchi discloses "it is possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and/or thickness of the resin coating *32* covering the conductive wire" (column 5, lines 29-33). Figures 8 and 9 clearly show a predetermined pattern and distance between the wires (42) with dielectric material (40) surrounding them. Horiuchi also teaches carefully selecting the dielectric material for the dielectric constant "and/or" thickness (column 5, lines 34-37). However, Horiuchi lacks disclosure of co-dispensing a plurality of bonding wires. Steranko discloses bonding multiple wires to a circuit board continuously (abstract, lines 1-9) as shown in figure 1. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the co-dispensing apparatus of Steranko in order to have strong bonding of multiple wires at one time (Steranko et al., column 1, lines 40-44).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Lee (US 2001/00154900 A1).

Horiuchi discloses bonding a plurality of bonding wires for signal transmission between and semiconductor chip (10) and a circuit board (5). However, Horiuchi lacks bonding a plurality of ribbon wires in the package. Lee teaches ribbon bonding wire for signal transmission (page 3, paragraph [0031], lines 3-10). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the bonding of ribbon bonding wire between the chip and circuit board in order to model transverse distribution adequately and utilize a wire-grid method to understand the influence of material during signal transmission (Lee, page 3, paragraph [0031], lines 6-10, and paragraph [0030}, lines 4-6).

Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Notani et al. (US 5, 924,897).

With respect to claim 15, Horiuchi lacks specific description of the bonding wires to comprise a microstrip. Notani discloses a transmission line having a microstrip line structure (column 7, lines 1-2). Regarding claim 17, it is understood that a microstrip transmits a single-ended signal as disclosed by the applicant. Therefore, Notani's disclosure of a transmission line having a microstrip structure (column 7, lines 1-2) satisfies a single-ended signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the disclosed microstrip of Notani in order to arrange the strip signal conductor opposite a ground conductor on the dielectric (Notani et al., column 7, lines 2-3).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 19 above, and further in view of Kurtz et al. (US 4,555,052).

The examiner interpreted high to be any value for dielectric constant of the insulating material due to the lack of relation to a low value and lack of specified values for a high dielectric constant. Horiuchi lacks disclosure of the particular material comprising the dielectric. However, Kurtz discloses ceramic as a dielectric material useful for electric insulation (column 6, lines 52-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the ceramic dielectric of Kurtz in order to properly bond the wire for transmission while the package is grounded (Kurtz et al., column 6, lines 47-52).

Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Grellmann et al. (US 4,686,492).

With respect to claim 31, Horiuchi lacks specific disclosure of both a signal current and a return current conducted by the plurality of bonding wires; however, Grellmann discloses a method for solving the inductive problem posed by wire bond connection in a configuration that essentially preserves the approximate predetermined impedance of the transmission line (Grellmann et al., col. 1, lines 55-60). Grellmann

also discloses a plurality of substantially co-planar layers of bond wires, each layer, comprising a signal-carrying line flanked on both sides therof by a ground line (col. 1, lines 64-67); thus, Grellmann's configuration of each signal line contains both signal and return currents. With respect to claim 32, Horiuchi lacks specific disclosure of the controlled impedance effect resulting from electromagnetic coupling amongst the bonding wires. However, Grellmann discloses the adjacent parallel layers being capacitive in order to compensate for the fundamentally inductive nature of the bond wire connection (col. 2, lines 4-15), and the impedance is therefore lower because the capacitance provided by the second bond wire layer (the configuration of the bonding wires) compensates for the inductive loading created by the first layer (col. 2, lines 29-32 and 37-40). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Horiuchi et al. to include the bonding wire configuration for controlling the impedance effect in the signal line of Grellmann et al. in order to provide an electrical connection between two electrical device utilizing conventional wire bonding techniques where the impedance of the wire bond matches the output/input impedances of the two electrical devices respectively (Grellmann et al., col. 2, lines 44-49).

Allowable Subject Matter

Claims 4, 14, 16, and 18 are objected to but would be allowable if the independent claim 1 was allowable.

Regarding claim 4, the prior art of record does not teach or suggest either alone or in combination all of the features of the method of making an electronic interconnection as claimed in claim 1 and including one of a first bonding wire and a second bonding wire of said plurality of wires is grounded.

Regarding claim 14, the prior art of record does not teach or suggest either alone or in combination all of the features of the method of making an electronic interconnection as claimed in claim 1 and including said bonding wires of said signal line comprise a combination of at least one round bonding wire and at least one ribbon wire.

Regarding claim 16, the prior art of record does not teach or suggest either alone or in combination all of the features of the method of making an electronic interconnection as claimed in claim 1 and including said plurality of bonding wires for said signal comprises a coplanar waveguide.

Regarding claim 18, the prior art of record does not teach or suggest either alone or in combination all of the features of the method of making an electronic interconnection as claimed in claim 1 and including said signal comprises a differential signal.

Claims 6, 21, and 22 are objected to but would be allowable if dependent claim 5 was allowable.

Regarding claim 6, the prior art of record does not teach or suggest either alone or in combination all of the features of the method of making an electronic

interconnection as claimed in claim 5 and including said dielectric material is periodically placed along the length of said plurality of bonding wires.

Regarding claim 21, the prior art of record does not teach or suggest either alone or in combination all of the features of the method of making an electronic interconnection as claimed in claim 5 and including a spacing of intervals of said particles permits an effect of one of a filter and an impedance transformer.

Regarding claim 22, the prior art of record does not teach or suggest either alone or in combination all of the features of the method of making an electronic interconnection as claimed in claim 5 and including a spacing of said dielectric material permits an effect of one of a filter and an impedance transformer.

Claims 28-30 are objected to but would be allowable if the independent claim 27 was allowable.

The prior art of record does not teach or suggest either alone or in combination all of the features of the method of providing a signal from a chip as claimed in claim 27 and including the controlled impedance designed to be near in value to at least one of an impedance of a circuit of said chip and an impedance of a circuit to which said signal line is interconnecting said chip circuit.

Response to Arguments

Applicant's arguments filed September 19, 2006 have been fully considered but they are not persuasive.

Applicant argues the finalized restriction requirement originally set forth in the restriction mailed on October 11, 2005. Applicant argues that the term "bonding wire" is a term of art that cannot be ignored in the restriction requirement analysis and it will be necessary for the USPTO to provide some evidence that such a plurality of bonding wires for a single signal line are used in an apparatus (pages 10-11). The examiner disagrees and reminds the applicant that a search of Group II, claims 25 and 26 (pertaining to "an electronic component") would require a search in class 438, subclass 26, which is not required for a search of Group I (process claims). Furthermore, the separate classification of the independent inventions of Groups I and II provides sufficient proof of serious burden on the examiner.

Applicant argues that "there are elements of the claimed invention which are neither taught nor suggested by Horiuchi, Notani, or newly-cited Kawai, when properly interpreted" (page 12). The examiner disagrees. Applicant's obvious concern over "proper" interpretation is in the eye-of-the-beholder and the "interpretation" of the claim is based on individual interpretation (which the examiner notes can be interpreted in many different ways by many different people). More importantly, the examiner "interprets" the claims with the broadest reasonable interpretation with respect to what one of ordinary skill in the art at the time of the invention would reasonably attain from the claim language. Thus, even if the examiner's interpretation differs from applicant's interpretation of the claim language, both interpretations are "proper" and applicant's argument that the examiner is not "properly" interpreting the claim language is moot. The applicant also argues that the obligation for broad interpretation is only for the claim

language and does not extend to the interpretation of the prior art references (page 12). The examiner agrees, and reminds the applicant that this exact approach has been used in the examination of the pending claims.

Applicant then argues that the rejections currently point to a plurality of bonding wires used for a plurality of signal lines, and does not point to the claim language of a plurality of bonding wires used for a single signal line (page 12). The examiner disagrees and reminds the applicant that Horiuchi (with respect to independent claim 1) discloses one signal line comprising a plurality of bonding wires (as claimed by the applicant). See column 5, lines 15-33. Applicant also argues that the rejections point to impedance effects in the prior art references, but none of these impedance effects are due to the configuration of a plurality of bonding wires for a specific signal line (page 12). The examiner disagrees. The applicant merely alleges that the prior art does not provide controlled impedance effects because of configuration without supporting this allegation by proving where the prior art teaches away from the applicant's claimed invention. With respect to claim 1 and the prior art of record, Horiuchi discloses the resin surrounding the bonding wires as part of the signal line and part of the reason for controlled impedance (Horiuchi et al, col. 5, lines 15-33). Therefore, the resin contributes to the "configuration" of the bonding wires and overall the "configuration" of the signal line, and it is reasonable to anticipate the broadly claimed limitation of claim 1. Applicant argues the examiner's interpretation of Kawai (page 13). However, this interpretation is moot in view of the new rejection, which no longer includes Kawai as prior art for rejection of the claim.

Applicant argues that "the prosecution history does not attempt to demonstrate a signal line that satisfies the plain meaning of this description and makes no attempt to explain what 'broadest reasonable interpretation' the examiner is giving the claim language" (page 13). The examiner disagrees, but in order to better explain the examiners position to the applicant and applicant's representative the examiner will clarify the interpretation of independent claim 1. As follows: "*A method of making an electronic interconnection*" has been interpreted exactly as it is broadly written and could include any and all methods which make any and all electronic interconnections within reason to one of ordinary skill in the art; "*method comprising: for a signal line to be interconnected*" has been interpreted any single signal line interconnected via the following limitation; "*using a plurality of bonding wires*" has been interpreted as the signal line must have a plurality of bonding wires conducting any signal (whether it be a signal, return, or ground current), and the bonding wires interconnect the signal line to be one whole functioning unit; "*configured to provide a controlled impedance effect*" has been interpreted to mean one of two broad interpretations including, (1) the signal line is configured to provide the controlled impedance effect, where configured can mean position, geometry, what it is connected to, or many of other features which provide any specific "configuration" of the line, or (2) the bonding wires are configured to provide the controlled impedance effect, where configured can mean many things including the spacing between wires, height raised from the bonding site, curvature of the wires between connection, placement of the wires, etc. The examiner reminds the applicant that the word "configuration" has been broadly interpreted, and no support or additional

limitations regarding the configuration (that is so important to the patentability of the instant invention) has been claimed in the independent claims in order to overcome the prior art currently of record.

Applicant also argues the "configuration of wirebonds in Kawai are not intended to provide a 'controlled impedance' effect in and of themselves" (page 14). The examiner notes that this argument is moot in view of the new rejection, which does not include Kawai as prior art with respect to the instant claim language. However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., configuration of wirebonds are intended to provide a controlled impedance effect in and of themselves) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). As stated above with respect to the examiner's interpretation of the broad claim limitation of instant claim 1, the claim does not specifically state that the wirebond configuration is the sole source of the controlled impedance effect ("in and of themselves"); but rather, the entire configuration of the signal line could control the effect as the claim is currently written. Applicants have not claimed any clear distinctions in the configuration of the wirebonds that could overcome Horiuchi (the current prior art of record with respect to the rejection of independent claim 1). Furthermore, as the inventors (Kwark and Schuster) suggested in the telephonic interview on August 16, 2006, their invention is distinguishable over prior techniques

because of the geometry and spacing of the wires in the single signal line; and because of this specific geometrical and special arrangements ("configurations") of the bonding wires in the signal line, there is a resulting controlled impedance effect. The examiner once again reminds the applicants that the independent claims, as they are currently written, do not clarify this position that the geometry and spacing (both features of a "configuration") of the bonding wires within a single signal line are the sole reason for this impedance effect.

The applicant argues that the "examiner seems to be confusing 'input and output' for 'signal' and 'return'" (page 14). First, the examiner is not "confusing" any claim limitation or features of the prior art; but the examiner is merely "interpreting" the claim language and applying relevant prior art, which anticipates or is obvious to arrive at the instant claim language as it is broadly claimed. Furthermore, this argument is irrelevant to the independent claims of the instant invention, because the newly amended independent claims have no mention of the configuration of the wires with respect to signal or return currents for providing the effect.

Applicant argues that the technique in primary references Horiuchi or Notani (or any of the prior art of record) fails to teach or suggest the method of the present invention of using a plurality of bonding wires configured to provide a controlled impedance effect (page 14). The examiner disagrees for all of the same reasons stated above with regard to the interpretation of the independent claims and lack of specificity of the configuration in order to overcome the primary references Horiuchi and Notani.

Also, applicant requests that the examiner point to a specific signal line in the prior art references, such that this signal line has a plurality of bonding wires that are configured to provide a controlled impedance effect (page 14). The examiner notes that this has been done in the rejection of the independent claims above, and more importantly the claims do not concede that the bonding wires are configured to provide a controlled impedance effect (noting the examiner's possible reasonable interpretation of the instant claim language that the configuration of the signal line as a whole could provide this effect). See the response to applicant's argument regarding "in and of itself" above. The examiner once again reminds the applicant that during patent examination, the pending claims must be "given the broadest reasonable interpretation." Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

Applicant then argues that other independent claims have similar claim language to that of claim 1 and therefore the same arguments as previously presented apply (page 15). The examiner therefore disagrees with the applicant's arguments regarding these claims for all of the same reasons as stated in response to applicant's arguments of claim 1 above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rachel E. Beveridge whose telephone number is 571-272-5169. The examiner can normally be reached on Monday through Friday, 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

reb
November 28, 2006

JONATHAN JOHNSON
PRIMARY EXAMINER